WHAT IS CLAIMED IS:

1. A nonvolatile semiconductor memory device comprising:

a floating gate electrode, formed on a semiconductor region, for storing carriers injected from said semiconductor region;

a control gate electrode for controlling a quantity of stored carriers by applying a predetermined voltage to said floating gate electrode; and

a source region formed in the semiconductor region on one of side regions of said floating gate electrode and control gate electrode and a drain region formed in the semiconductor region on the other of the side regions thereof;

wherein said drain region creates an electric field so that the carriers injected to said floating gate electrode are subject to an external force having an element directed from said semiconductor region to said floating gate electrode.

2. A nonvolatile semiconductor memory device comprising:

a floating gate electrode formed on a semiconductor region via a first dielectric film;

a control gate electrode capacitively coupled with said floating gate electrode via a second dielectric film; and

a source region and a drain region that are formed in

said semiconductor region on side regions of said floating gate electrode and control gate electrode;

wherein the end of said drain region faced with said source region has an embedded drain region extending toward said source region without reaching the surface of said semiconductor region, and

a channel region is formed near the surface of said semiconductor region above said embedded drain region in.

3. The nonvolatile semiconductor memory device according to claim 2, further comprising an embedded region adjacent upper area that is formed in an upper part of said embedded drain region in the semiconductor region and has a conduction type opposite to that of said drain region.

4. The nonvolatile semiconductor memory device according to claim 3, wherein an impurity concentration in said embedded region adjacent upper area is higher than that in said semiconductor region.

5. The nonvolatile semiconductor memory device according to claim 3, wherein said embedded drain region has a conduction type opposite to that of said drain region and an impurity concentration lower than that in said embedded region adjacent upper area.

6. The nonvolatile semiconductor memory device according to claim 2, wherein said embedded drain region has the same conduction type as that of said drain region and an impurity concentration lower than that in

said drain region.

7. The nonvolatile semiconductor memory device according to claim 2, further comprising an embedded region adjacent lower area that is formed in the lower part of said embedded drain region in said semiconductor region and has a conduction type opposite to that of said drain region.

8. The nonvolatile semiconductor memory device according to claim 7, wherein an impurity concentration in said embedded region adjacent lower area is higher than that in said semiconductor region.

9. The nonvolatile semiconductor memory device according to claim 2,

wherein said semiconductor region has a stepped portion,

said floating gate electrode is formed astride said stepped portion, and

said drain region and embedded drain region are formed under a lower side of the said stepped portion.

10. The nonvolatile semiconductor memory device according to claim 2, wherein the carriers located in said channel region under said floating gate are subject to a force element of the electric field perpendicular to the surface of said semiconductor region when a predetermined voltage is applied to said control gate electrode or said drain region.

11. The nonvolatile semiconductor memory device according to claim 2, wherein said control gate

electrode is formed above said floating gate electrode.

12. The nonvolatile semiconductor memory device according to claim 2, wherein said control gate electrode is formed on said semiconductor region in the vicinity of the side of said floating gate electrode.

13. A nonvolatile semiconductor memory device manufacturing method comprising the steps of:

forming an embedded drain region by injecting a first impurity in a semiconductor region so that a top of said embedded drain region does not reach the main surface of said semiconductor region;

forming a gate dielectric film on the main surface of said semiconductor region;

forming first and second gate electrodes on said gate dielectric film so that the first gate electrode capacitively coupled with the second electrode is located above said embedded drain region; and

injecting a second impurity into said semiconductor region, using said first and second gate electrodes as masks, to form a source region in said semiconductor region on one of side regions of the first and second gate electrodes, and a drain region in the other of the side regions thereof under said first gate electrode so that it contacts said embedded drain region.

14. The nonvolatile semiconductor memory device manufacturing method according to claim 13, further comprising the step of forming an embedded region

adjacent upper area above a formation region to be formed as said embedded drain region in said semiconductor region by selectively injecting a third impurity having a conduction type opposite to that of said second impurity into said semiconductor region prior to the formation of said gate electrode.

15. The nonvolatile semiconductor memory device manufacturing method according to claim 13, further comprising the step of forming an embedded region adjacent lower area under a foramtion region to be formed as said embedded drain region in said semiconductor region by selectively injecting a third impurity having a conduction type opposite to that of said second impurity into said semiconductor region prior to the formation of said gate electrode.

16. The nonvolatile semiconductor memory device manufacturing method according to claim 13, wherein the step of forming said gate electrode includes the step of forming said second gate electrode above said first gate electrode via a capacitance dielectric film.

17. The nonvolatile semiconductor memory device manufacturing method according to claim 13, wherein the step of forming said gate electrode includes the step of forming said first gate electrode on the side of said second gate electrode via a capacitance dielectric film.

18. The nonvolatile semiconductor memory device manufacturing method according to claim 13, further

comprising the step of forming a stepped portion above a formation region to be formed as said embedded drain region in said semiconductor region prior to said gate dielectric film formation step, so that the lower stage of said stepped portion is the side of said drain region, wherein said first gate electrode is formed astride said stepped portion in said gate electrode formation step.

19. The nonvolatile semiconductor memory device manufacturing method according to claim 13, further comprising the step of forming a stepped portion above a formation region to be formed as said embedded drain region in said semiconductor region prior to said embedded drain region formation step, so that the lower stage of said stepped portion is the side of said drain region, wherein said first gate electrode is formed astride said stepped portion in said gate electrode formation step.

20. The nonvolatile semiconductor memory device manufacturing method according to claim 13, wherein the conduction type of said first impurity is the same as that of said second impurity and the concentration of said first impurity is lower than that of said second impurity.

21. The nonvolatile semiconductor memory device manufacturing method according to claim 14, wherein the conduction type of said first impurity is different from that of said second impurity and the concentration of

said first impurity is lower than that of said third impurity.